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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,104	10/10/2001	Warren Snyder	CYPR-CD00183	8786

7590 06/16/2006

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/975,104	SNYDER, WARREN	
	Examiner	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 17* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's RCE application, filed on 04/11/2006. Claims 1-2, 4-13, and 15-17 are pending in the Action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 , 4-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over. Barnett et al, US patent no. 6,173,419 B1, in view of Marantz et al, US patent no. 6,061,511.

As per claim 1, Barnett anticipates an emulation method and emulator for debugging a target circuit with feature limitations very identical to the claimed invention. According to Barnett, the emulation method includes steps

Executing a sequence of instructions by a device under test, wherein the device under test comprises a data line and a clock line (col. 5, lines 7-30),

Executing the sequence of instructions by an emulator device emulating the function of the target circuit or device under test in lock-step manner with the device under test for real time debugging and improving the quality data transfer by locking input/output data for channel synchronization (Figs. 7 and 8, col. 5, lines 30-46, col. 6, line 33 to col. 7, line 10),

Conveying I/O read information from the device under test to the emulator device over the data line during a data transfer (col. 6, line 33 to col. 7, line 62),

A host computer system reading real time state and debug information from the emulator device without interrupt the device under test (cols. 5-7). Barnett does not expressly disclose a feature of "the emulator device shares a clock signal with the device under test". Such claimed limitation is however well-known in the art. In fact, Marantz teaches a clock share between emulator and device under design (DUT) (col. 7, lines 25-51, col. 8, lines 29-60) to trace internal net for logic transition (col. 1, lines 5-10, col. 3, lines 12-25, for example)

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of clock share between the emulator and DUT as in Marantz into the Barnett in order to trace and debug logic in the internal net as taught in Marantz above.

As per claim 2, Barnett discloses the emulation in a cycle comprises data transfer and a control phase for an integration of emulation data.

As per claim 4, Barnett discloses an I/O transfer mechanism as claimed for synchronization, for instance.

As per claims 5-8 and 13, Barnett discloses the device under test having a plurality of data lines as claimed, each claimed line could have a number of bits for information transmission as claimed (col. 6, line 51 to col. 7, line 10).

As per claim 9, Barnett discloses an emulation method and emulator for debugging a target circuit with feature limitations very identical to the claimed invention. According to Barnett, the emulation method includes steps

Executing a sequence of instructions by a device under test, wherein the device under test comprises a data line and a clock line (col. 5, lines 7-30),

Executing the sequence of instructions by an emulator device emulating the function of the target circuit or device under test in lock-step manner with the device under test for real time debugging and improving the quality data transfer by locking input/output data for channel synchronization (Figs. 7 and 8, col. 5, lines 30-46, col. 6, line 33 to col. 7, line 10),

Conveying I/O read information from the device under test to the emulator device over the data line during a data transfer (col. 6, line 33 to col. 7, line 62),

A host computer system reading real time state and debug information from the emulator device without interrupt the device under test (cols. 5-7), and conveying interrupt vectors or breakpoints from the microcontroller to the emulator device during an interrupt service cycle (cols. 5-7). Barnett does not expressly disclose a feature of "the emulator device shares a clock signal with the device under test". Such claimed limitation is however well-known in the art. In fact, Marantz teaches a clock share between emulator and device under design (DUT) (col. 7, lines 25-51, col. 8, lines 29-60) to trace internal net for logic transition (col. 1, lines 5-10, col. 3, lines 12-25, for example)

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of clock share between the emulator and DUT as in Marantz into the Barnett in order to trace and debug logic in the internal net as taught in Marantz above.

As per claim 10, Barnett discloses the emulation in a cycle comprises data transfer and a control phase within the cycle for data integrity.

As per claims 11 and 12, Barnett discloses an I/O transfer mechanism such as data transfer during emulation as claimed for timing and synchronization, for instance.

As per claim 15, Barnett discloses breakpoints of interrupt service cycles for data assertion.

Allowable Subject Matter

Claims 16 and 17 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the claims are directed to a method of obtaining debug information for emulation of the device under test. The method requires steps "executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT. wherein said emulator device shares a clock signal with said DUT"; "the DUT and the emulator device operating in a cycle comprising a data transfer phase and a control phase, wherein I/0 read information is conveyed to the emulator device during the data transfer phase after a start of instruction transition occurs and prior to execution of an instruction"; wherein "the I/O read information comprises eight bits of information, and

wherein the I/O read information is conveyed to the emulator device over said two data lines carrying four serial bits each over a time period defined by four system clock cycles; and conveying interrupt vectors from the DUT to the emulator device during an interrupt service cycle, with the interrupt service cycle begins after assertion of an interrupt data line". Because the prior art does not teach the limitations as shown in claims 16 and 17, the claims are allowed.

Response to Arguments

Applicant's arguments with respect to claims1-2 , 4-13, and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,134,516, issued to Wang et al, on Oct. 2000
2. US patent no. 6,732,068 B2, issued to Sample et al, on May 2004
3. US patent no. 6,934,674, issued to Douezy et al, on Aug. 2005

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 12, 2006

Thai Phan
Patent Examiner